Overview

This lab will introduce students to modular design techniques; Testbench file simulations, and Vivado’s I/O planning tool for pin constraints.

Students will learn how to:

- Create modular designs
- Design a Testbench file to verify Input/Output behavior
- Use Vivado’s I/O planning tool to set pin constraints

Preliminary Work

Download the provided Testbench file from the course website

Lab Work

1. Carefully read and follow the lab 1 tutorial.
2. Using what you have been shown in the tutorial, design a Testbench file for the Full Adder design and 2-bit Full Adder design. Then show the simulation results.
3. Program the ZYBO with the completed 2-bit Full Adder design and verify its functionality using the following inputs.

   11 + 00
   11 + 01
   11 + 10
   11 + 11
   01 + 01